

15750 U.S. PTO  
022704

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Leonard Forbes et al.

Title: INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD

Attorney Docket No.: 1303.024US2

Customer No.: 21186

PATENT APPLICATION TRANSMITTAL

**MAIL STOP PATENT APPLICATION**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following attached items and information (as indicated with an "X"):

- ☒ Return postcard.
- ☒ **DIVISIONAL** of prior Patent Application No. (09/945,498) (under 37 CFR 1.53(b)) comprising:
- ☒ Specification (48 pgs, including claims numbered 1 through 40 and a 1 page Abstract).
- ☒ Formal Drawing(s) (15 sheets).
- ☒ Copy of signed Declaration (5 pgs) from prior application.
- ☒ Copy of Power of Attorney from prior application (1 pg).
- ☒ Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
- ☒ Check in the amount of \$1388.00 to pay the filing fee.
- ☒ Prior application is assigned of record to Micron Technology, Inc.
- ☒ Information Disclosure Statement ( 2 pgs), Form 1449 ( 5 pgs )  
References NOT enclosed, cited in prior application.
- ☒ Communication Concerning Related Applications (2 pgs.).

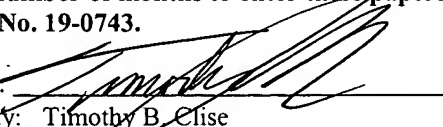
The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	40-20	20	x 18.00 =	\$360.00
INDEPENDENT CLAIMS	6-3	3	x 86.00 =	\$258.00
[] MULTIPLE DEPENDENT CLAIMS PRESENTED				\$0.00
BASIC FEE				\$770.00
TOTAL				\$1388.00

Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers. Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number: 21186

By:   
Atty: Timothy B. Clise  
Reg. No. 40,957

"Express Mail" mailing label number: EV370240261US

Date of Deposit: February 27, 2004

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.

16434 U.S. PTO  
10/789038  
022704

**S/N Unknown**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Leonard Forbes et al.	Examiner:	Ly D. Pham
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	Herewith	Docket:	1303.024US2
Title:	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD		

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**COMMUNICATION CONCERNING RELATED APPLICATION(S)**

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/945395	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945498	August 30, 2001	1303.024US1	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: Unknown

Filing Date: Herewith

Title: INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD

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10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
<i>Not Available</i>	February 20, 2004	1303.019US2	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
<i>Not Available</i>	February 18, 2004	1303.063US2	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicants' Representatives,

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